## REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

### I. Disposition of Claims

Claims 1-13 are pending in the present application. Claims 1, 7, and 8 are independent. The remaining claims depend, directly or indirectly, from claims 1, 7, and 8.

### II. Objection(s) to the Specification

The Specification was objected to as containing various informalities. By way of this reply, paragraphs [0006], [0009], [0011], [0032], and [0033] of the Specification have been amended to correct any informalities. Accordingly, withdrawal of the objection to the Specification is respectfully requested.

### III. Rejection(s) under 35 U.S.C § 103

*Claims 1, 2, 8, and 9*

Claims 1, 2, 8, and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson ("Resonance and Damping in CMOS Circuits with On-Chip Decoupling Capacitance," Patrik Larsson, IEEE Transactions on Circuits and Systems, August 1998, pages 849-858) in view of U.S. Patent No. 6,240,246 issued to Evans (hereinafter "Evans") and U.S. Patent No. 3,808,370 issued to Jackson et al. (hereinafter

"Jackson"), and further in view of U.S. Patent Application Publication No. 2002/0011885 in the name of Ogawa et al. (hereinafter "Ogawa") and Herrell et al. ("Modeling of Power Distribution Systems for High-Performance Microprocessors," Dennis J. Herrell and Benjamin Baker, IEEE Transactions on Advanced Packaging, August 1999, pages 240-248). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for modeling an anti-resonance circuit of a microprocessor. The technique uses a load model that simulates the anti-resonance circuit, a transistor that simulates at least one high-frequency capacitor, and a capacitor that simulates an intrinsic capacitance of a section of the microprocessor. Further, the transistor and capacitor are connected in parallel with the load model.

As discussed with reference to an exemplary embodiment of the present invention shown in Figure 8 of the present application, the model, representing a physical section of a chip, includes a load **86** (representing a load model for that section of the chip) that is connected in parallel to a transistor $C_{local}$ **88** and a voltage-controlled capacitor $C_{intrinsic}$ **90**. The load model may be a voltage controlled resistor (see, e.g., paragraph **[0034]**). $C_{local}$ **88** and $C_{intrinsic}$ **90** represent local high-frequency capacitors and the intrinsic transistor capacitance of the section of the chip, respectively. The values of each load **86**, transistor $C_{local}$ **88,** and capacitor $C_{intrinsic}$ **90** are selected to accurately simulate the performance of its specific modeled component (see, e.g., paragraph [**0034**]).

The modeling of an anti-resonance circuit of a microprocessor in accordance with the present invention provides low complexity with a simulation time that may be orders of magnitude faster than a model that uses transistors. Further, the model provides flexibility in accurately modeling system performance in AC analysis (see, e.g.,

paragraph [**0037**]).

Larsson discloses the use of a model to predict the resonance frequency of a CMOS circuit (see, e.g., page 849, col 2, para 1, lines 1-7). Through the use of a model, Larsson simplifies a complex CMOS circuit into RC networks and further to a simple second-order system in order to estimate the resonance frequency of the circuit (e.g., page 857, col. 1, para 2, lines 1-4). Larsson also proposes design techniques to control resonance and increase damping in a CMOS circuit (e.g., page 849, col 1, para 3, lines 11-13). However, Larsson is silent with respect to discussion of an anti-resonance circuit of a microprocessor. Larsson does not disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, where the capacitor is connected in parallel with the load model.

Evans discloses a device for filtering feedback signals available in an electromechanical actuation system (e.g., col. 1, lines 16-19). In Evans, a method for filtering oscillations in a closed loop control system for controlling the movement of a structure is disclosed. Evans is completely silent with respect to modeling a circuit, and specifically with respect to an apparatus that models an anti-resonance circuit of a microprocessor. Like Larsson, Evans does not disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance

of a section of the microprocessor, where the capacitor is connected in parallel with the load model. Accordingly, Evans fails to disclose all of the limitations of independent claim 1, or to provide that which Larsson lacks.

The Applicant further notes that there is no motivation or suggestion to combine the teachings of Larsson with Evans. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the prior art references themselves (MPEP § 2143). Regardless of whether prior art references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art, *not* in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

The Examiner indicates that it would have been obvious to one skilled in the art to modify the apparatus of Larsson including an apparatus for modeling a resonance circuit of a microprocessor with the apparatus of Evans that included an anti-resonance mixing filter circuit. However, the device of Evans is used to control the **movement of a structure** that amplifies displacement oscillations when operating at resonant frequencies (see, e.g., col. 1, lines 50-54), while Larsson uses a model to predict the **resonance** frequency of a CMOS circuit. Clearly, these two devices are not combinable.

As discussed above, Larsson uses a model to predict the resonance frequency of a

CMOS circuit. Larsson is silent with respect to modeling an anti-resonance circuit of a microprocessor. Jackson is directed to a system using adaptive filters for detecting formant information in speech and in determining pitch and/or anti-resonance information (col. 1, lines 47-51). Jackson cannot be combined with Larsson.

Jackson references U.S. Patent No. 3,190,963, which clearly states that in voice applications, antiresonant frequencies correspond to regions of relatively ineffective transmission through a talker's vocal tract (col. 1 lines 48-50). Thus, the anti-resonant information of Jackson has no connection to the present invention. Jackson states that an object of the invention disclosed therein is to determine pitch or anti-resonance information, but this relates to voiced speech. Jackson provides no motivation for modeling an anti-resonance circuit of a microprocessor.

Like Larsson and Evans, Jackson does not disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, where the capacitor is connected in parallel with the load model, as required by the claimed invention, or provide that which Larsson and Evans lack.

The Examiner stated that Jackson teaches a transistor that simulates at least one high frequency capacitor, but the Applicant respectfully notes that the subject material and the citations correspond more appropriately to Ogawa, as Jackson does not contain a number of the listed citations. For example, the citation listed as Page 23, Para 0229, does not exist in Jackson, but appears to correspond to Ogawa. Regardless, the

Examiner's assertion that either reference teaches the simulation of at least one high-frequency capacitor is incorrect.

Ogawa discusses a transistor description format that allows the internal circuit configurations of a large scale integrated circuit to be accurately described with transistor models, interconnection resistance models, and capacitance models (see, e.g., page 1, Para 0007, lines 7-11). Ogawa does not discuss simulating a high-frequency capacitor with a transistor. Further, like Larsson, Evans, and Jackson, Ogawa does not disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, where the capacitor is connected in parallel with the load model, as required by the claimed invention, or provide that which Larsson, Evans, and Jackson lack.

The Examiner states that Herrell teaches that the transistor is connected in parallel with the load model (Page 240, Col. 1, Para 1, L1-7; Page 240, Col. 2, Para 2, L1-7; Page 241, Col. 1, Para 2, L1-3; Page 241, Col. 2, Para 1, L1-4; Page 241, col. 2, Fig. 2), as this allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, Col. 2, Para 1, L1-4). However, in Figure 2, Herrell merely shows a simplified circuit with essential features of a microprocessor power delivery system. Like Larsson, Evans, Jackson, and Ogawa, Herrell does not disclose, or otherwise teach, (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor

that simulates an intrinsic capacitance of a section of the microprocessor, where the capacitor is connected in parallel with the load model, as required by the claimed invention, or provide that which Larsson, Evans, Jackson, and Ogawa lack.

In view of the above, Larsson, Evans, Jackson, Ogawa, and Herrell, whether considered separately or in any combination, fail to disclose all the limitations of independent claims 1 and 8 of the present application. Additionally, there is no motivation to combine the references contained within the references themselves.

Moreover, the application of these **five** unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from **five** different references to achieve the claimed invention. In view of the lack of any teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

Thus, in view of at least the above, independent claims 1 and 8 of the present application are patentable over the above references. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

*Claims 3 and 10*

Claims 3 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable

over Larsson in view of Evans and Jackson, and further in view of Ogawa, Herrell, and U.S. Patent No. 4,459,566 issued to Lane (hereinafter "Lane").

Like the above cited references, Lane fails to disclose all the limitations of independent claims 1 and 8 of the present application or supply that which the above references lack. It is asserted that Lane teaches that the resistor is a voltage controlled resistor (page 9, section 8.1). This is not correct. The device of Lane is a voltage controlled **oscillator** (VCO) (see, for example, col. 1, lines 51-62). A VCO, as explained by Lane, provides an output signal having a **frequency** proportional to the magnitude of an input control signal.

Therefore, like Larsson, Evans. Jackson, Ogawa, and Herrell, Lane fails to disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, where the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model, as required by independent claims 1 and 8 of the present application. Accordingly, because independent claims 1 and 8 have been shown to be patentable, claims 3 and 10 are allowable for at least the same reasons.

The Applicant further notes that there is no motivation to combine the teachings of Lane with Larsson, Evans, Jackson, Ogawa, and Herrell. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the

prior art references themselves (MPEP § 2143). Regardless of whether prior art references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). Further, the present application *cannot be used as a guide* in reconstructing elements of prior art references to render the claimed invention obvious. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art." *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

Moreover, the application of these **six** unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from **six** different references to achieve the claimed invention. In view of the lack of any teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

*Claims 4, 5 11, and 12*

Claims 4, 5, 11, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Ogawa, Herrell, and U.S. Patent No. 6,370,678 issued to Culler (hereinafter "Culler").

Like the previously cited references, Culler fails to disclose all the limitations of

independent claims 1 and 8 of the present application or supply that which the others lack. The device of Culler uses circuit simulations on models of power supply circuits to determine the primary resonant frequencies identified with each of the power supply circuits. These resonant frequencies are used as input to the initial floor planning (Col. 4, lines 53-59). Culler discloses that these models and the identification of resonant frequencies can be used to develop design constraints supplied as input to the logic synthesis process (see abstract). There is no disclosure in Culler of anti-resonance circuit designs for microprocessors.

Therefore, like Larsson, Evans, Jackson, Ogawa, and Herrell, Culler does not disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, where the capacitor is connected in parallel with the load model, as required by independent claims 1 and 8 of the present application. Accordingly, because independent claims 1 and 8 have been shown to be patentable, claims 4, 5, 11, and 12 are patentable for at least the same reasons.

The Applicant further notes that there is no motivation to combine the teachings of Culler with Larsson, Evans, Jackson, Ogawa, and Herrell. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the prior art references themselves (MPEP § 2143). Regardless of whether prior art

references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art." *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

Moreover, the application of these **six** unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from **six** different references to achieve the claimed invention. In view of the lack of any teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

*Claims 6 and 13*

Claims 6 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Ogawa, Herrell, Culler, and U.S. Patent 5,223,653, issued to Kunimoto et al. (hereinafter "Kunimoto").

Like Larsson, Evans, Jackson, Ogawa, Herrell, and Culler, Kunimoto does not disclose, or otherwise teach, at least (i) a load model that simulates an anti-resonance circuit of a microprocessor, (ii) a transistor that simulates at least one high frequency

capacitor, wherein the transistor is connected in parallel with the load model, and (iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, where the capacitor is connected in parallel with the load model, as required by independent claims 1 and 8 of the present application. Further, Kunimoto does not teach that a load model begins to simulate an anti-resonance circuit on the leading edge of a clock cycle, as asserted by the Examiner (Fig. 1; Col. 1, L29-37; Col. 5, L35-37).

Thus, it is unclear why one skilled in the art would combine the device of Kunimoto with Larsson, Evans, Jackson, Ogawa, Herrell, and Culler. The invention of Kunimoto relates to a musical tone synthesizing apparatus that is suitable for synthesizing a percussion instrument tone. Kunimoto is directed to a device that simulates and synthesizes a percussion instrument tone with a closed loop including at least an adder and a delay circuit (see abstract). Thus, the device of Kunimoto is clearly not combinable with the above cited references.

The Applicant further notes that there is no motivation to combine the teachings of Kunimoto with Larsson, Evans, Jackson, Ogawa, Herrell, and Culler. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the prior art references themselves (MPEP § 2143). Regardless of whether prior art references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). The teaching or suggestion to make the claimed combination and the reasonable expectation of success

must *both* be found in the prior art. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

Moreover, the application of these **seven** unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from **seven** different references to achieve the claimed invention. In view of the lack of any teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

*Claim 7*

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Culler. For the reasons set forth below, this rejection is respectfully traversed.

Claim 7 is a means-plus function claim requiring a means for simulating an anti-resonance circuit and a means for synchronizing the means for simulating an anti-resonance circuit with a clock signal. The Examiner has rejected claim 7 based on similar reasoning to the rejections of claims 1 and 4. Therefore, for at least the reasons discussed with respect to claims 1 and 4, independent claim 7 is patentable over Larsson, Evans, Jackson, and Culler. Larsson, Evans, Jackson, and Culler, whether taken independently or in combination, fail to show or suggest the present invention as recited

in independent claim 7. Accordingly, withdrawal of this rejection is respectfully requested.

**IV. Conclusion**

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/065001; P5347).

Respectfully submitted,

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